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A 12-Bit High Speed Analog To Digital Convertor Using µp 8085

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ABSTRACT
The need constantly exists for converters with higher resolution, faster conversion speeds and lower power dissipation. High-speed analog to digital converters (ADC's) have been based on flash architecture, because all comparators sample the analog input voltage simultaneously, this ADC is thus inherently fast. Unfortunately, flash ADC requires 2^N - 1 comparators to convert N bit digital code from an analog sample. This makes flash ADC's unsuitable for high-resolution applications. This paper demonstrates a simple technique to enhance resolution of flash ADC's that require as few as 256 comparators for 12-bit conversion. In this approach, the analog input range is partitioned into 256 quantization cells, separated by 255 boundary points. An 8-bit binary code 00000000 to 11111111 is assigned to each cell. A 12-bit flash converter requires 4096 comparators, while proposed technique reduces number of comparator requirements to only 256 for 12- bit conversion. Therefore, this technique is best suitable when high speed combined with high resolution is required. Result of 12-bit prototype is presented.

Keywords: Flash ADC, µP, DAC, Sample and Hold. Successive approximation.

I. INTRODUCTION

Digital control systems are extensively used in the field of motion control. High performance digital control systems have created a need for high speed and high resolution analog to digital converters (ADC's) with extremely wide dynamic range. Typically, high-resolution ADC's have been based either on self-calibrated successive approximation [1-3] or over sampling architectures [4, 5]. However, both of these architectures are unsuitable for high-speed applications. Flash ADC's are typical choice for high-speed applications. However, The Parallelism of the flash architecture has drawbacks for higher resolution applications. The number of comparators grows exponentially with N [6], in addition, the separation of adjacent reference voltages grows smaller exponentially, and consequently this architecture requires very large IC's. It has high power dissipation. Two-step Flash converters are popular for conversion resolutions in the 8-12 bit range where optimized designs can achieve low power dissipation and small silicon area for implementation [7, 8]. However, beyond such resolution, the area and power dissipation of two-step flash ADC's nearly double for each additional bit of resolution [9].

There are many different architectures like pipelined convertor [10, 11], successive approximation convertor [12, 13], Sigma-Delta convertor [14], folding ADC's, reported recently for high-speed applications. Nevertheless, these architectures have significant amount of complexity. In this paper, a simple technique is proposed to enhance resolution of flash ADC's. The prototype ADC based on this technique uses only 256 comparators instead of 4096 comparators normally required in the flash ADC's for 12-bit resolution.

II. ADC ARCHITECTURE

The ADC based on proposed technique enjoys the benefit of employing only 256 comparators instead of 4096 comparators normally required in conventional 12-bit flash architecture while maintaining the advantage of high speed. The block diagram of the 12-bit ADC using proposed technique is illustrated in Fig. 1. The ADC consists of an 8-bit flash ADC, 12-bit DAC, 8-bit µP 8085, 2-PPI 8255 and some extra supporting circuit blocks. 8-bit flash ADC, partitions input range into 256-quantization cells. From the 8-bit code µP decides within which cell the input sample lies. 12-bit code for that cell is obtained by successive approximation technique.

III. CIRCUIT IMPLEMENTATION

The block diagram of the 12-bit ADC is as shown in Fig. 1. The 8255-I port A is used as input port, which gets the 8-bit code from 8-bit flash

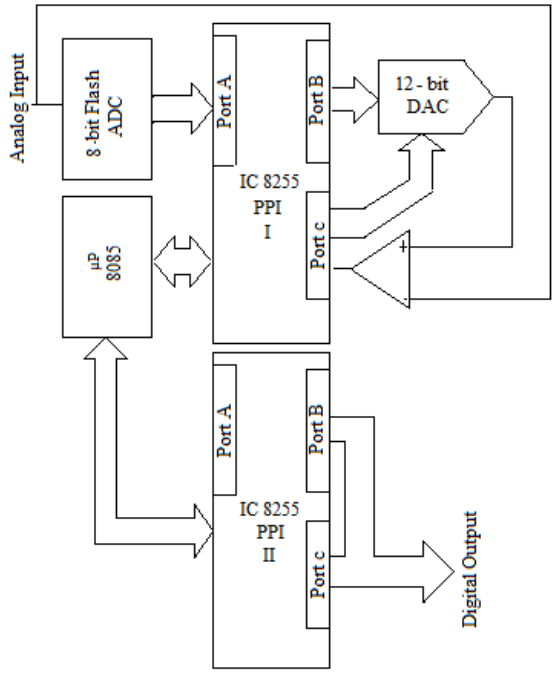

Figure 1: Block diagram of 12-bit ADC

ADC, corresponding mid value 12-bit binary code of a particular cell is loaded into the accumulator. Port B and Port C upper of 8255-I is used as output ports, connected to 12-bit DAC through to obtain analog signal equivalent to digital count in register A, which is compared with an analog input voltage V_{IN}. Equivalent 12-bit digital code for analog input signal is obtained by successive approximation technique. The conversion algorithm is similar to the binary search algorithm. First, the reference voltage of a particular cell, $V_{ref\ (DAC)}$ provided by DAC is set to $V_N / 2$ to obtain the MSB, where V_N is the maximum cell voltage of a particular cell and N is cell number. After getting the MSB, successive approximation convertor moves to the next bit with $V_N/4$ or $3/4*V_N$ depending on the result of the MSB. If the MSB is "1", then $V_{ref(DAC)} = ¾*V_N$, otherwise $V_{ref(DAC)} = V_N/4$ This sequence will continue until the LSB is obtained.

Fig. 2 shows how the reference voltages are implemented for analog signal sample lies in the third cell ($V_3/2$=038H). Note that $15/16*V_3$ (03FH) is the largest reference voltage and $1/16*V_3$ (030H) is the smallest reference voltage. To get a 12-bit digital output, four comparisons are needed. Finally 12-bit digital code is available at Port B and Port C of PPI 8255-II.

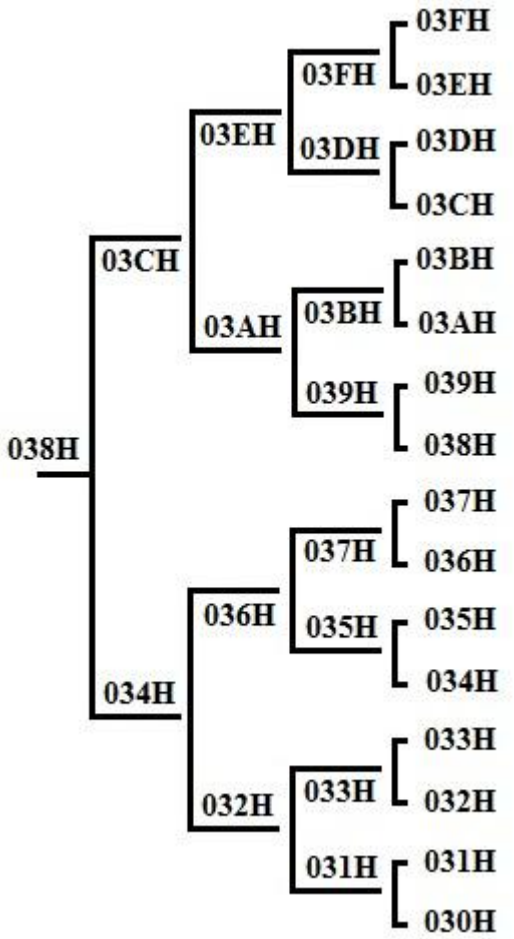

Figure 2: Reference voltage tree in successive Approximation technique

Software for implementing successive approximation converter in µP is written in assembler code and converted to hex code by assembler software.

IV. MEASURED RESULT

An experimental prototype of 12-bit ADC using proposed technique was designed and developed using µP8085. The working functionality of the ADC has been checked by generating a ramp input going from 0 to 5V (full scale range of the ADC). Digital codes have been obtained correctly, going from 0 to 4095 for 12-bit at the output, indicating that the ADC's working is functionally correct.

Both the differential and integral nonlinearities (DNL and INL) were measured over 2^{12} output codes by applying slowly varying full scale range ramp as input to the proposed ADC, which completes the full scale range in 4095 steps .The values of the each code are compared with ideal value and store the difference value. The results show that the ADC exhibits a maximum DNL of 0.52 LSB and a maximum INL of 0.55LSB as shown in the Figs. 3(a) and 3(b).

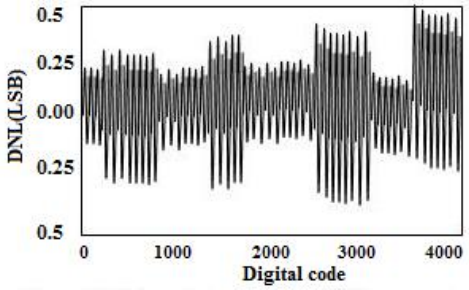

Figure 3(a): Differential Non Linearity Versus output Code

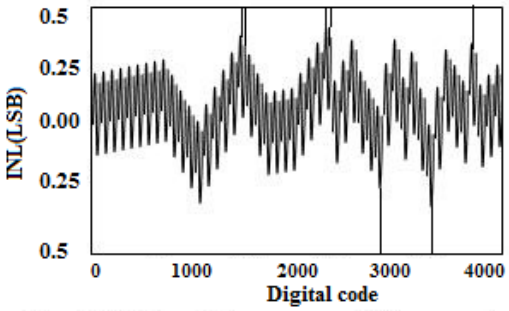

Figure 3(b): Integral Non Linearity Versus output Code

V. CONCLUSION

We have presented a simple and effective technique for enhancing resolution of 8-bit flash ADC. This technique would be effective in a large number of high-speed controls and signal processing applications such as hard-disk-drive read Chanel and wireless receivers. Although these applications are most often implemented with flash convertors, but these ADC's demands larger power. Also, the ADC die area and power dissipation increase exponentially with resolution, limiting the resolution of such ADC's less than 10bits. The main conclusion is that although Flash convertors provide high conversion rates, required power dissipation of these ADC's are large. Also, resolution beyond 10-bits these ADC's become prohibitively expensive and bulky. Proposed technique provides high enough conversion speed for high-speed applications, with less power dissipation even beyond 10-bit resolution. Implementation of successive approximation algorithm using µP 8085 has reduced the hardware requirement and cost. Proposed technique uses only 256 comparators for 12-bit resolution.

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